

- FPGA design
- ASIC design
- IP licensing



industry 4.0



healthcare



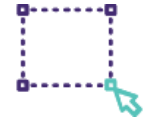
space



reliable



high
performant



scalable



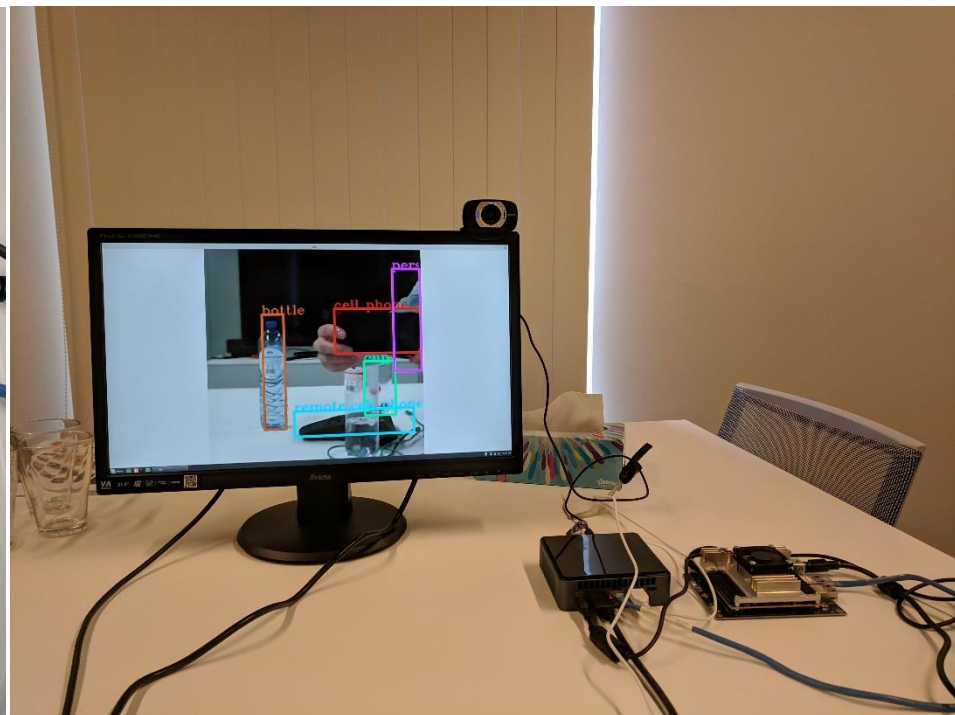
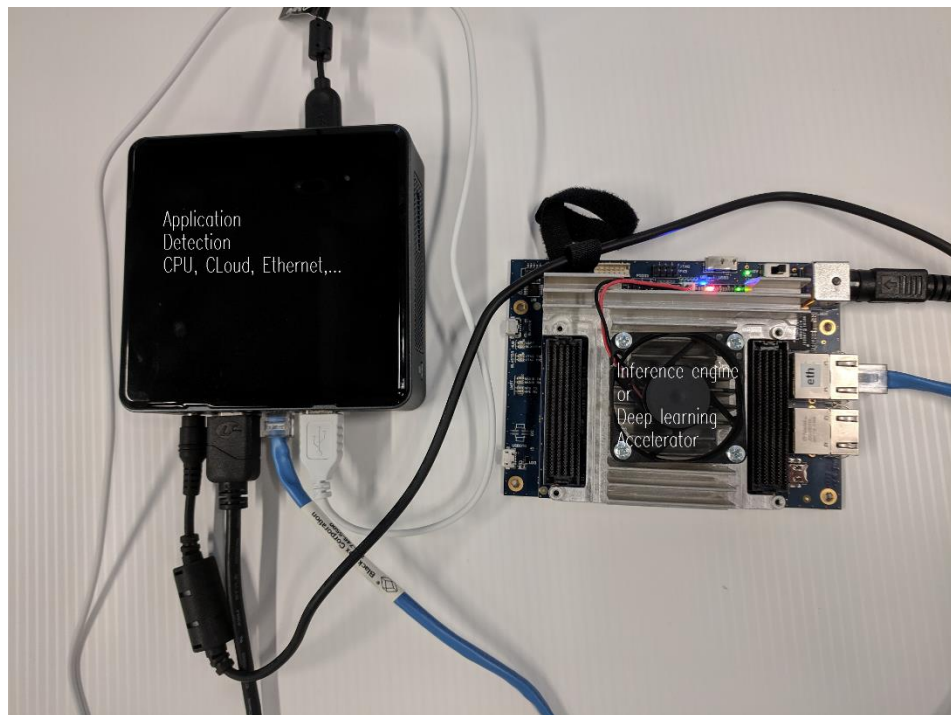
low-power



Deep learning in a box

- ▶ Embed deep learning in your application!





Autonomous driving

Vision:
Quality Inspection

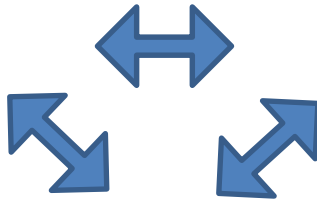
Smart city & Retail

Agriculture

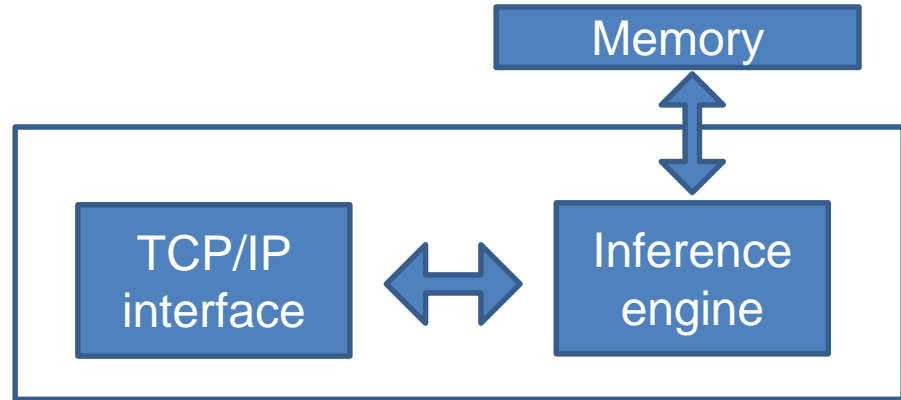
Robotics

Sensor Data

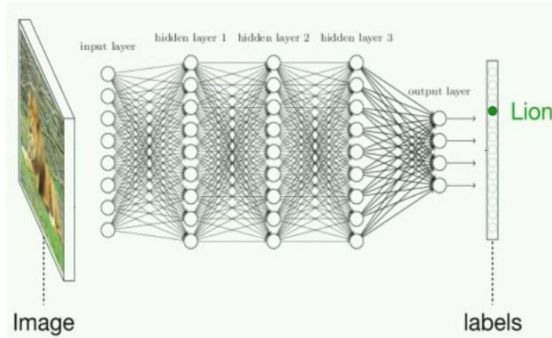
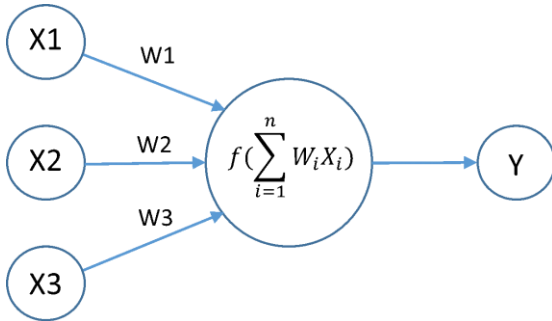
- 2D image sensors
- 3D image sensors
- Event based sensors
- Lidar
- IR
- Hyperspectral
- ToF
- Audio
- Radar



Application CPU



matrix processor specialized for neural network work loads



0	0	0	0	0	0
0	105	102	100	97	96
0	103	99	103	101	102
0	101	98	104	102	100
0	99	101	106	104	99
0	104	104	104	100	98

Image Matrix

Kernel Matrix

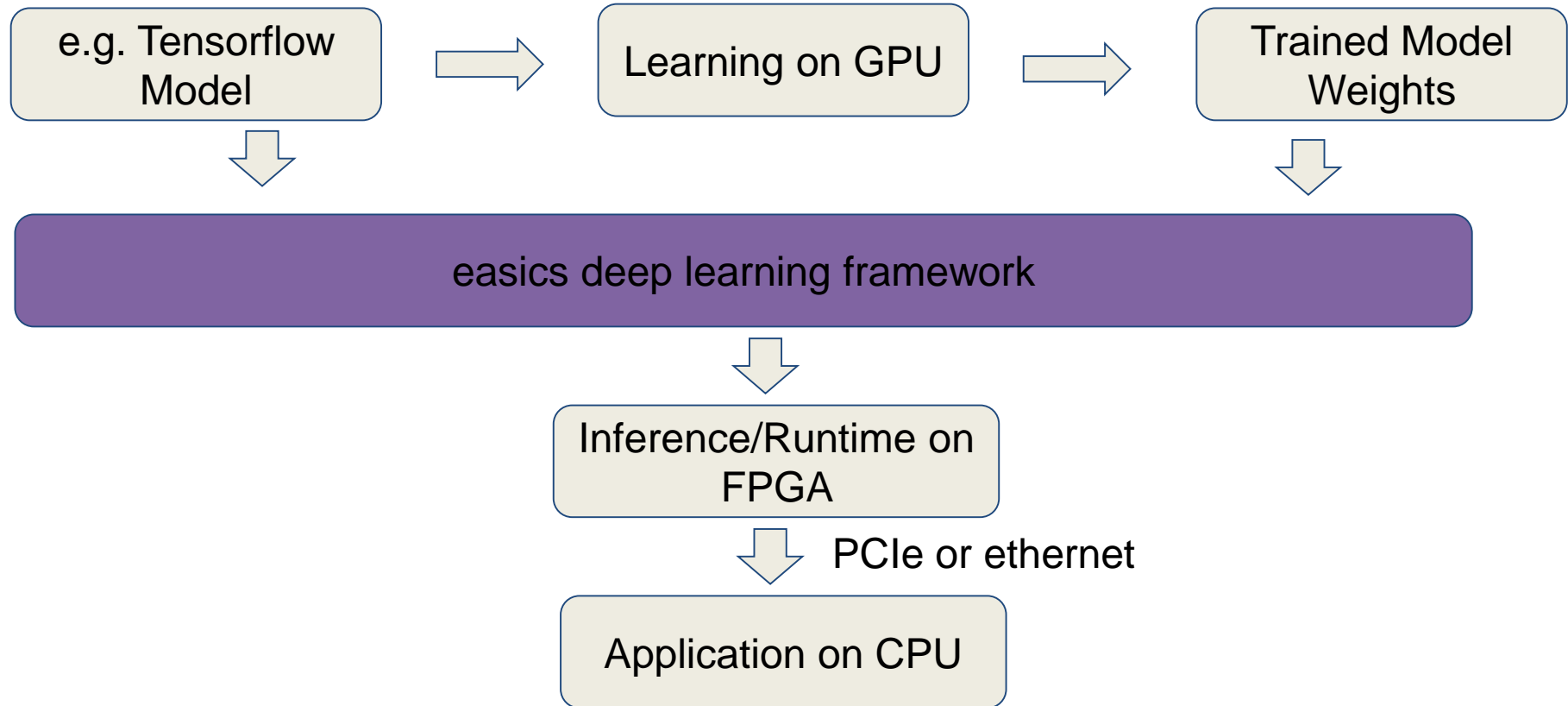
0	-1	0
-1	5	-1
0	-1	0

320				

Output Matrix

$$\begin{aligned}
 & 0 * 0 + 0 * -1 + 0 * 0 \\
 & + 0 * -1 + 105 * 5 + 102 * -1 \\
 & + 0 * 0 + 103 * -1 + 99 * 0 = 320
 \end{aligned}$$

Convolution with horizontal and vertical strides = 1

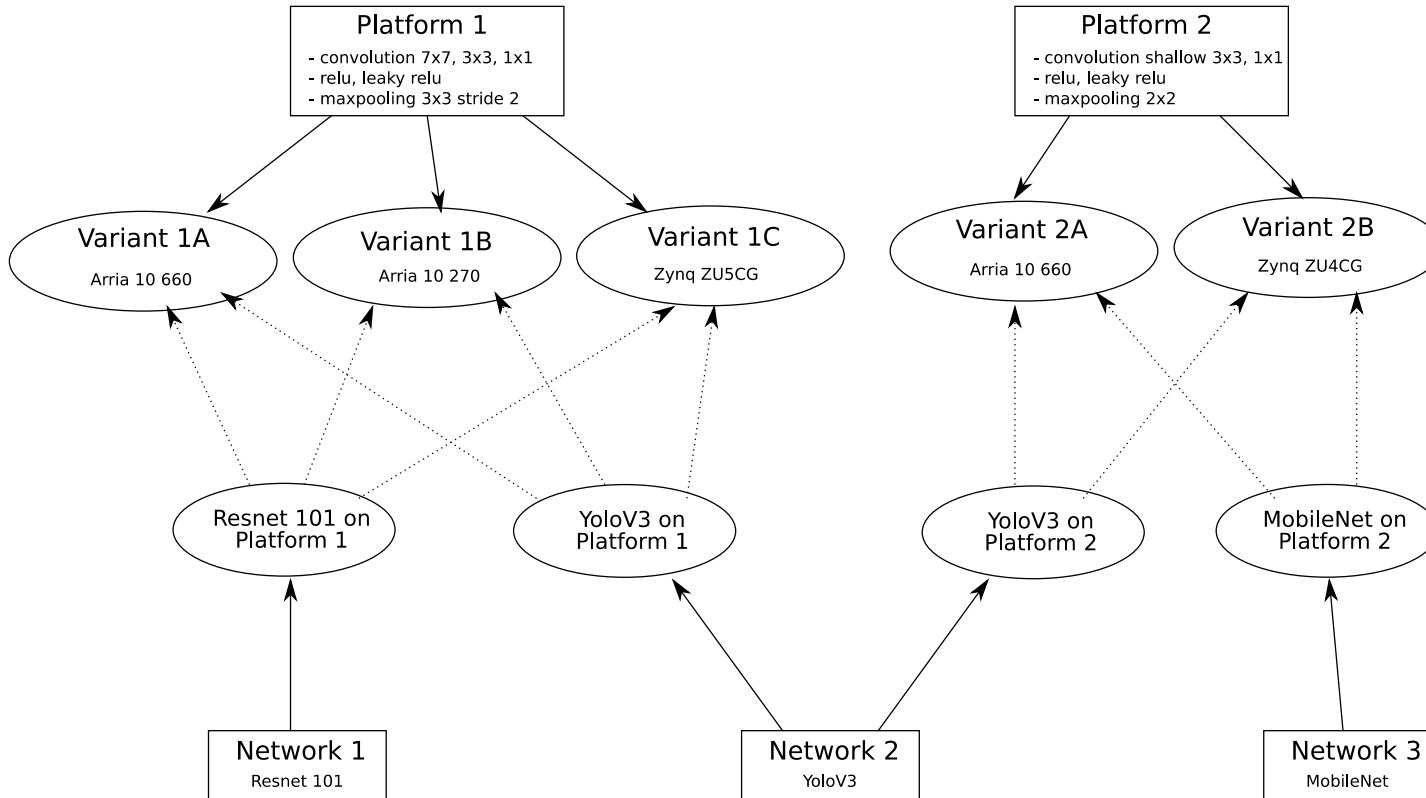


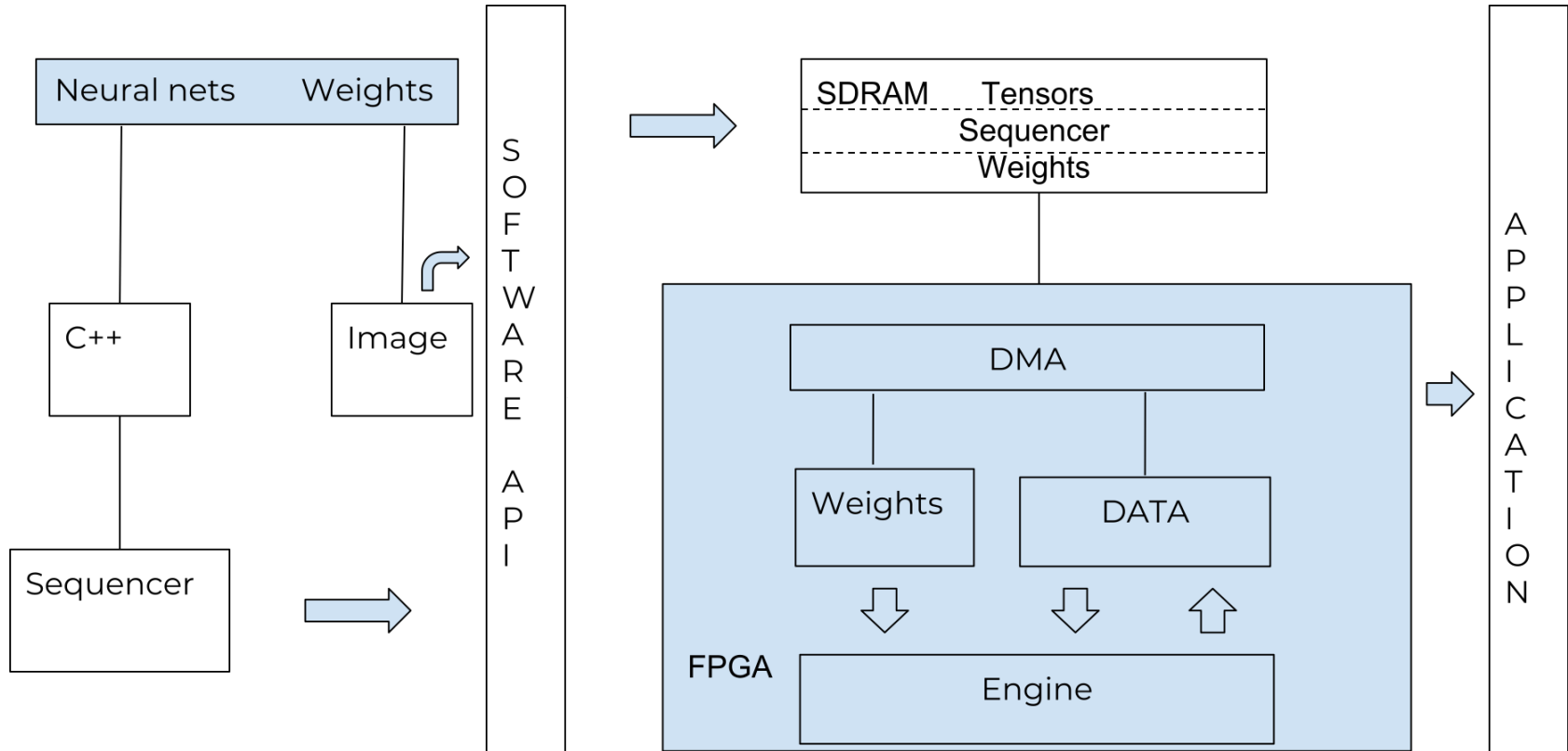
Implementation

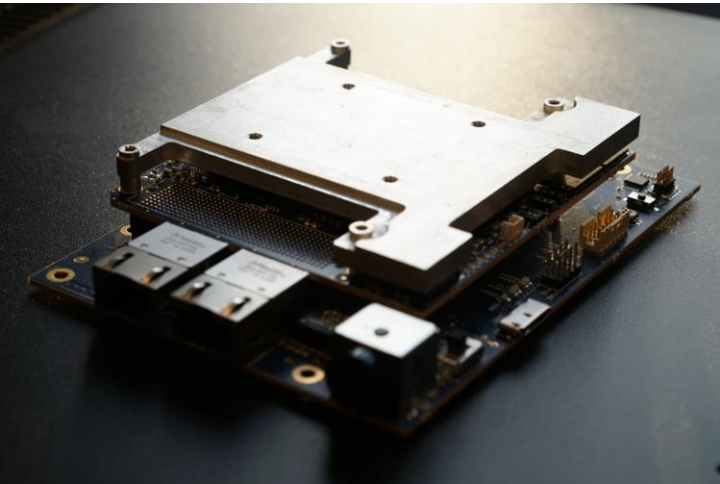
Configuration +
assisted implementation

Generation

Assisted
Implementation



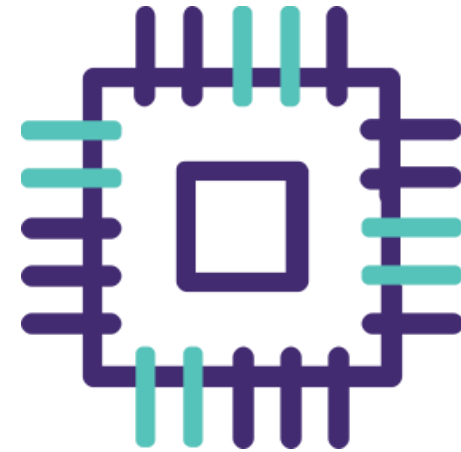




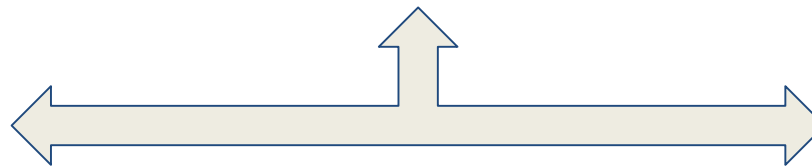
Deep learning in a Box

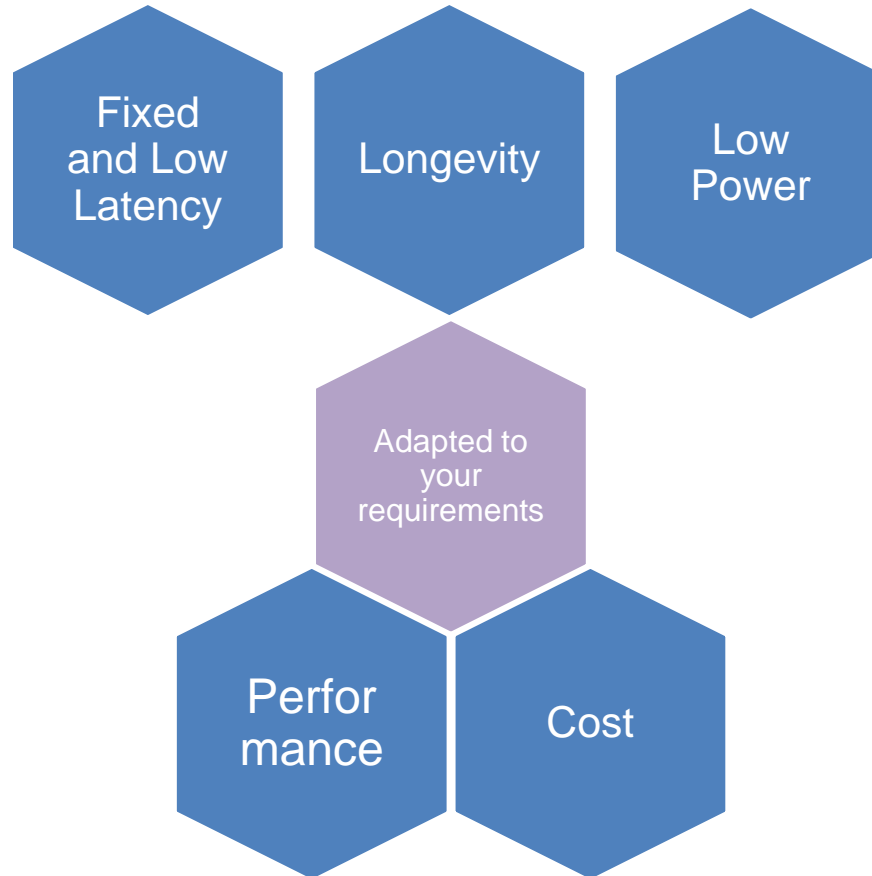


FPGA



ASIC







Located at the Arenberg science park in Leuven



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